CLAIMS

What is claimed is:

1. A method comprising:

(a) receiving a periodic signal, the periodic signal having periodic signal cycles with corresponding time durations, wherein the time durations of the periodic signal cycles are substantially identical;

(b) generating a control signal having a magnitude, the magnitude of the control signal varying smoothly over a plurality of the periodic signal cycles; and

(c) delaying the periodic signal and thereby generating an output signal, wherein the output signal has output signal cycles with corresponding time durations, and wherein each of the time durations of the output signal cycles is a function of the magnitude of the control signal during the time duration.

2. The method of claim 1, wherein the delaying in (c) is performed by a variable delay element.

3. The method of claim 1, wherein the magnitude of the control signal is current.

4. The method of claim 1, wherein the periodic signal is received from an external oscillator.

5. The method of claim 1, wherein the output signal is a spread spectrum clock signal.

6. The method of claim 1, wherein the output signal is generated without using a phase locked loop.

7. The method of claim 1, wherein the magnitude of the control signal increases exponentially over a plurality of the periodic signal cycles.

8. The method of claim 1, wherein the magnitude of the control signal varies in a quasi-sinusoidal manner over a plurality of the periodic signal cycles.

9. The method of claim 1, further comprising, between (a) and (b):

(d) generating an intermediary signal with a magnitude, wherein the magnitude of the intermediary signal varies substantially linearly over a plurality of the periodic signal cycles and is generated by an analog integrator, and wherein the magnitude of the control signal varies in substantially an exponential manner over the plurality of the periodic signal cycles.

10. The method of claim 9, wherein a non-linear signal is generated from the intermediary signal by a non-linear signal generator, and wherein the control signal is generated from the non-linear signal by a current mirror.

11. A method comprising:

(a) supplying a periodic signal onto a data input lead of a variable delay element, the variable delay element also having a data output lead and a control input lead, wherein a propagation delay through the variable delay element from the data input lead to the data output lead varies as a function of a magnitude of a control signal on the control input lead; and

(b) varying the magnitude of the control signal smoothly over a length of time that encompasses a plurality of cycles of the periodic signal, the varying of the magnitude of the control signal causing an output signal to vary smoothly in frequency over the length of time, the output signal being output onto the data output lead.

12. The method of claim 11, wherein the magnitude of the control signal increases exponentially over the length of time.

13. The method of claim 11, wherein the magnitude of the control signal varies in a quasi-sinusoidal manner over the length of time.

14. The method of claim 11, wherein the magnitude of the control signal is a voltage magnitude.

15. The method of claim 11, further comprising:

(c) generating the control signal by dividing the periodic signal.

16. A device comprising:

a counter portion that receives a periodic signal and outputs a divided signal, the periodic signal having periodic signal cycles with corresponding time durations;

an integrator that receives the divided signal and outputs a signal having a magnitude; and

a variable delay element that receives the periodic signal and outputs an output signal, wherein the output signal has output signal cycles with corresponding time durations, and wherein each of the time durations of the

output signal cycles is a function of the magnitude of the signal output by the integrator during the time duration.

17. The device of claim 16, further comprising:

a non-linear signal generator that receives the signal output by the integrator and generates a non-linear signal having a magnitude, wherein each of the time durations of the output signal cycles is a function of the magnitude of the non-linear signal during the time duration.

18. The device of claim 17, wherein the magnitude of the non-linear signal is a voltage magnitude.

19. The device of claim 16, wherein the variable delay element receives a control signal having a magnitude, and wherein each of the time durations of the output signal cycles is substantially proportional to the magnitude of the control signal during the time duration.

20. The device of claim 19, wherein the magnitude of the control signal is a current magnitude.

21. A device comprising:

a counter portion that receives a periodic signal having periodic signal cycles with corresponding time durations; and

means for generating (i) a control signal having a magnitude that varies smoothly over a plurality of the periodic signal cycles and (ii) an output signal having output signal cycles with corresponding time durations, wherein the output signal is generated by delaying the periodic signal, and wherein each of the time durations of

the output signal cycles is proportinal to the magnitude of the control signal during the time duration.

22. The device of claim 21, wherein the magnitude of the control signal is a current magnitude.

23. The device of claim 21, wherein the means does not include a voltage controlled oscillator.

24. The device of claim 21, wherein the output signal is a spread spectrum clock signal.

25. A device comprising:

a variable delay element that receives a periodic signal and a control signal and outputs an output signal, wherein the periodic signal has a periodic signal cycle with a corresponding time duration, wherein the control signal has a control signal cycle with a corresponding time duration, a corresponding slope and a corresponding DC offset, wherein the output signal has an output signal cycle with a corresponding time duration, and wherein the time duration of the output signal cycle is a function of the time duration, the slope and the DC offset of the control signal during the time duration of the periodic signal cycle; and

a programmable spread spectrum control register with a first plurality of bits, a second plurality of bits and a third plurality of bits, wherein the first plurality of bits controls the DC offset of the control signal cycle, the second plurality of bits controls the slope of the control signal cycle, and the third plurality of bits controls the time duration of the control signal cycle.

26. The device of claim 25, further comprising:
a counter portion that receives the periodic signal.

27. The device of claim 25, wherein the control signal is generated by dividing the periodic signal.

28. The device of claim 25, wherein the periodic signal cycle is one of a plurality of periodic signal cycles, wherein the control signal has a magnitude, and wherein the magnitude of the control signal varies smoothly over the plurality of the periodic signal cycles.

29. The device of claim 28, wherein the magnitude of the control signal is a function of the time duration, the slope and the DC offset of the control signal.

30. The device of claim 25, wherein upon powering up the device, the first plurality of bits, the second plurality of bits and the third plurality of bits are set such that the time duration of the output signal cycle is substantially identical to the time duration of the periodic signal cycle.

31. The device of claim 25, wherein the device does not include a phase locked loop.

32. An integrated circuit comprising:

a processor;

an input lead;

a spread spectrum clock generator that receives a clock signal from the input lead and outputs a delayed clock signal to the processor; and

a programmable bit that is writable by the processor, wherein if a first digital logic value is stored in the programmable bit then the delayed clock signal has a substantially constant frequency, and wherein if a second digital logic value is stored in the programmable bit then the delayed clock signal has a variably dithered frequency.

33. The integrated circuit of claim 32, wherein the integrated circuit is a microcontroller integrated circuit.